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LETTER TO THE EDITOR

Electronic instabilities in the hot-electron regime of the one-dimensional ballistic resistor

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Abstract. We provide evidence for both voltage- and current-controlled negative differential resistance instabilities in the one-dimensional ballistic resistor driven into the hot-electron regime. Quantum reflections are used to explain the former effect, while extra electron sub-bands provide the current 'filaments' in the latter case.

The quantisation of the one-dimensional ballistic resistance [1, 2] and related phenomena [3, 4] have been extensively investigated recently. The experiments have used high-mobility two-dimensional electron gases (2DEGs) narrowed into one-dimensional (1D) channels by the electrostatic action of a negative bias applied to 'split gates' [5] in structures that are suitable adaptations of the high-electron-mobility transistor. In all these experiments, a very small source–bias, typically a few microvolts, is applied. The low-field resistance is quantised, taking values of $h/(2ne^2)$, i.e. $12.9/n$ kΩ, where n is an integer, being the number of one-dimensional sub-bands occupied by electrons in the 1D channel, the factor of two arising from spin degeneracy.

We have recently considered the regime of high source–drain bias, typically up to 100 mV, representing a potential energy change for a ballistic electron that is up to 10 times the Fermi energy ($E_F \simeq 10$ meV) of the 2DEG contacts to the 1D channel. On the basis of the simple Landauer formula [6] for the resistance, we predict a form of voltage-controlled (or so-called N-type, as the current–voltage characteristics have an N shape) negative differential resistance (NDR) based on quantum reflection once the source–drain bias exceeds E_F/e. It is the evidence for this form of NDR, and evidence of a current-controlled NDR (or the so-called S-type) that we describe here. The more detailed theory and the device implications of the voltage-controlled NDR are described elsewhere [7, 8].

The structure on which these experiments have been performed (see figure 1(a)) consists of a GaAs/AlGaAs heterojunction (grown by molecular beam epitaxy) containing a 2DEG of carrier density 2.75×10^{11} cm^{-2} (hence the E_F cited above), and a 4 K low-field mobility of 0.98×10^6 cm^2 V^{-1} s^{-1}. After using optical lithography to define a mesa, conventional source and drain Ohmic contacts were added. The Schottky gate

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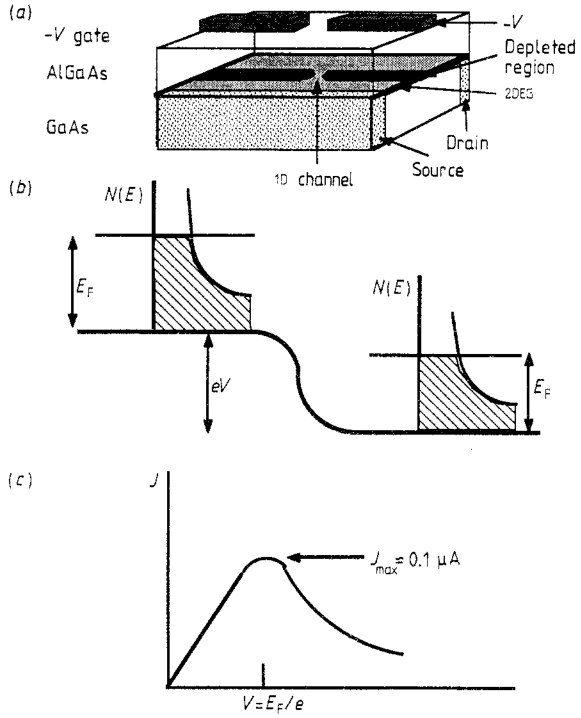

Figure 1. (*a*) A schematic diagram of the active region of the device, (*b*) a diagram of the relevant electron states, noting that in 1D, $N(E) \sim 1/\sqrt{E}$, and (*c*) the inferred current–voltage characteristic.

consists of a metal line, 0.3 μm wide, bisecting the mesa between source and drain. A split in this gate is 0.3 μm wide, and the two sections are connected off-mesa. In the experiments the gate is biased negatively with respect to the source, typically by 0.5–5 V, the lower value being sufficient to deplete carriers from underneath the gate and so define the 1D channel, while the upper value is sufficient to pinch off the channel entirely. With a low source–drain bias, we see first a steady rise in resistance as the channel is defined, and successive quantised resistance plateaux as the channel is progressively narrowed by the action of the split gate bias.

Using a simple zero-temperature model for the current in a single 1D electron sub-band we write, (cf figure 1(*b*)), for the current going from left to right

$$J_{\rightarrow} = e \int N(E)\, v(E)\, |t(E)|^2 f(E)(1 - f(E + eV))\, \mathrm{d}E$$

where $v(e)$ is the velocity of electrons of energy E, $N(E)$ is the 1D density of states $(= 2/hv(E)$, with the 2 for spin), $t(E)$ is the (complex) transmission coefficient for an electron incident from the left and $f(E)$ is the Fermi occupation factor. The limits of integration are from 0 to E_F, representing the range of energies of filled initial states: a similar argument gives $J_{\leftarrow}$. For small biases $|t(E)| = 1$ to high accuracy. The net current at low temperatures, and for a small bias, comes from the contribution to the integral for $J_{\rightarrow}$ between the limits $E_F - eV$ and E_F. The quantised resistance follows directly from the integration giving $J = 2e^2V/h$. Once eV exceeds E_F, the lower limit of the integral remains at zero, so that if $|t(E)|$ remains equal to unity, a current saturation would follow.

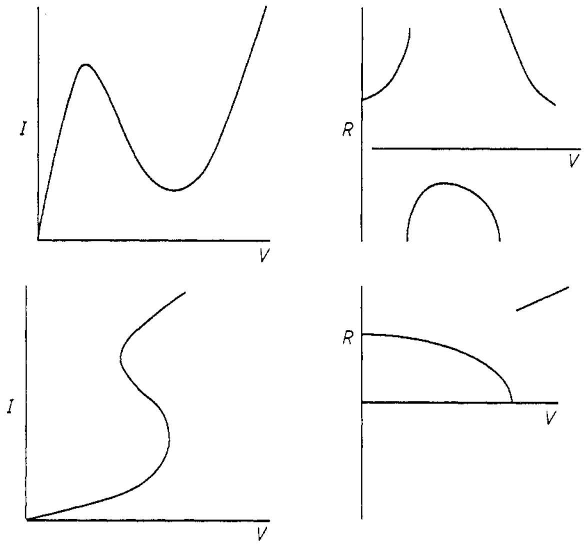

Figure 2. The current–voltage characteristics, and the associated differential resistance, for (*a*) N-type or voltage-controlled and (*b*) S-type or current-controlled electron instabilities.

In fact it is possible [7] to calculate the $t(E)$ for several simple models of the source–drain bias profile within the 1D channel: note that since the 2DEG has a resistance of $\leqslant 1\ \mathrm{k}\Omega$, most of the voltage is dropped along the 1D channel in our experiments. The result of this calculation is that $|t(E)|$ drops from unity as the bias increases, reaching about 0.95 for incident energy of order E_F with a bias of E_F/e applied, and as small as about 0.7 for $eV = 10\ E_F$. The relative effect increases for smaller incident energies. The precise shape of $t(E,V)$ depends on the potential profile, but the decrease in $t(E)$ with V is general. If we add this $t(E)$ factor into the equation for $J_{\rightarrow}$ we arrive at a $J(V)$ characteristic given in figure 1(*c*), showing NDR for bias greater than E_F/e.

Note that the differential resistance should increase, passing through $+\infty$ near E_F/e before increasing from $-\infty$ (see figure 2). In practice, while such NDR is manifest as circuit instabilities caused by the formation of high-field regions [9], we should be able to observe a rise in differential resistance at low to moderate biases. In practice, there are several 1D sub-bands acting in parallel, each with a different value of E_F relative to the minimum sub-band energy, and we would expect the effects described above to be more prominent near the condition of pinch-off where few sub-bands are occupied. All sub-bands will be in the N-type NDR regime when eV exceeds the Fermi energy in the lowest-energy sub-band. However, the precursor rise in the differential resistance may be masked in the multi-sub-band case, with the fact that some channels are in the NDR regime as a given channel approaches its maximum current level.

The N shape of the J–V characteristic is in contrast to the S shape that occurs when current instabilities are caused by parallel current filamants [9]. (Again see figure 2.) A similar analysis of the characteristic shows that the differential resistance in this case falls, reaching zero at the point where the current filaments occur. In the experiments described in greater detail below, the gate is biased negative with respect to the source: we then measure the differential resistance as a function of source–drain bias. A negative drain potential complements the gate bias in confining the layers by raising slightly the bottom of the conduction band at the constriction with respect to its value in the absence of a source–drain bias. Conversely a positive drain potential works against the gate bias and effectively deepens the channel, and in this case we can allow one or more extra 1D electron sub-bands to become occupied as the drain bias increases. These extra sub-bands in turn carry current for the same drain bias, i.e. they act as the current filaments required of S-type NDR. The precise voltage scale on which this instability occurs is now a function of the geometry of the device and the relative source and gate biases, and the overall effect does not depend on the relative Fermi energies in different sub-bands. The precursor fall in differential resistance should be more pronounced for S-type NDR; there is no degree of internal cancellation from the different sub-bands as in the N-type NDR.

We now consider experiments that show evidence of both forms of NDR, both from the precursor properties of the differential resistance, and the subsequent current–voltage instabilities. The experimental arrangements are as follows: once the gate has been biased negatively with respect to the (earthed) source, to define the 1D channel, the drain is then biased with respect to the source as required. This bias is obtained by passing a constant DC current through the device. A small AC signal ($I_{AC} = 10$ nA) is then superimposed on the DC current and the differential resistance of the 1D channel and 2DEG contacts is measured using standard phase-sensitive detection techniques. Four terminals are employed to avoid measuring the Ohmic contact resistance; however, the DC bias is measured across the whole device including the source and drain contacts as this was found to reduce greatly the noise in the measuring circuit. All of the experiments reported here are for a temperature of 4.2 K. The constant currents (both AC and DC) are produced by applying the required voltage at one terminal of a large resistance (1 MΩ) that is connected at the other end to the sample drain. The different DC biases are then obtained by sweeping the DC voltage source while the AC is kept at a constant magnitude. A standard plot is obtained by fixing the gate voltage, thereby holding the channel width constant (until the effect of the drain bias is taken into account) and then sweeping the DC bias.

In figure 3, we show differential resistance data for a range of gate voltages as the source–drain voltage, V_{SD}, is swept both positive and negative. We see that provided $|V_{SD}| \geqslant 20$ mV, there is noise in the differential resistance not present when $|V_{SD}| < 20$ mV. This we attribute to the onset of the N-type NDR of the form described above. We note, particularly in the traces for $V_g = -1$ V and -1.5 V that there is an asymmetry in the differential resistance at low bias, consistent with S-type NDR in forward bias and N-type in reverse. The asymmetry is masked in both (i) the $V_g = -0.5$ V case where the channel is barely defined, and (ii) the $V_g = -1.75$ V case near pinch-off where only one lateral sub-band is occupied: with the high resistance value in this case, the simple argument in the earlier paragraph on the interaction of gate and drain biases probably needs refinement.

Four questions remain: (i) why does the measured differential resistance rise to the high values when $|V_{SD}| > 50$ mV, (ii) what is the precise nature of the charge instabilities and related circuit oscillations in each case, (iii) what is the precise relation between V_g and V_{SD}, and (iv) how general is the effect we have observed?

The rise in the magnitude of the differential resistance at higher bias follows from the point of inflection in the J–V curve in figure 1(c) at a bias of approximately $2E_F/e$, beyond which the magnitude of the differential resistance increases. The data thus confirm the qualitative form of the J–V curve.

We are in a transport regime never examined before. At 10^{-7} A, and with a channel about 0.3 μm long, only a few electrons are in each channel of the device at any time.

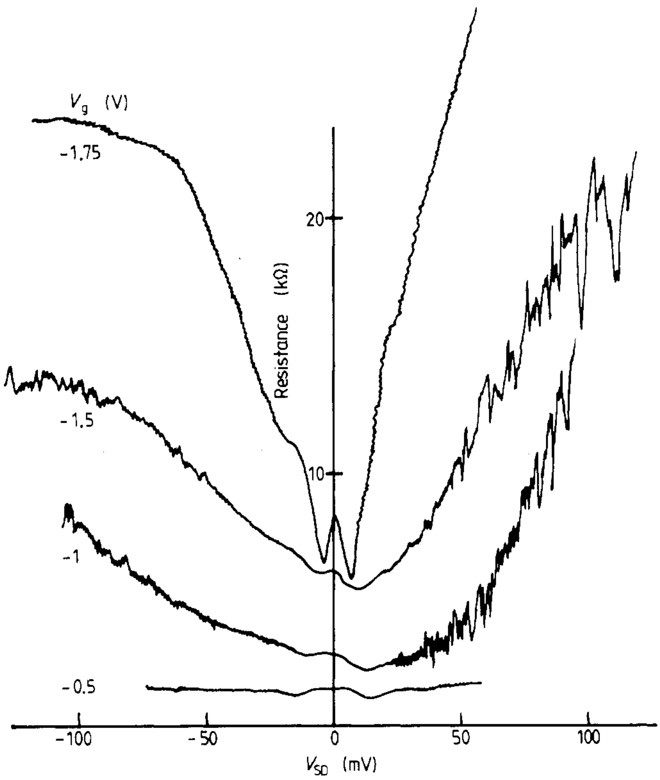

Figure 3. The differential resistance, as a function of source–drain bias, for a number of values of gate voltage. The channel narrows as the gate voltage is swept negative.

The current density, at $\sim 10^7$ A m^{-2} is relatively low in comparison with other diode structures. Most of the types of electric field and current instabilities already considered for other negative differential resistance mechanisms are not appropriate here (except possibly the uniform field mode of transferred electron devices [9]). A systematic series of pulse response measurements with varying circuit reactances will be required to establish the modes of instability.

The quantisation of the ballistic resistance relies on the inelastic mean free path being much longer than the device feature size. This length is likely to drop once phonon emission becomes possible from the heated electrons. We have seen no evidence for any reduction in the basic NDR effect that might result from a feedback from inelastic scattering of the heated electrons to an increased transmission coefficient. The several sub-bands seem to operate in parallel, with no evidence for interaction. At elevated temperatures and higher fields the inter- and intra-sub-band scatterings are likely to play a more important role.

The fact that both V_g and V_{SD} interfere to produce the actual shape of the potential in the constriction, and in our case the S-type NDR in forward bias, comes from the form in which the source contact is grounded. The N-type NDR should be seen more clearly, and be symmetric with source–drain bias, if the gate voltage is fixed with respect to the average of the source and drain potential, and the geometry of the device is symmetric between source and drain about the gate.

The requirements for NDR as described above are a condition of current saturation from a limited suppply of carriers, and quantum reflection at a strongly varying potential. Even the 1D density of states is not required in the current saturation; any integrable form of density of states up to the Fermi energy will suffice, provided only that the geometry allows a significant change in the potential on the scale of the electron wavelength, which varies upwards from about 0.05 μm at the Fermi energy of the lowest-energy sub-band. However, if the channel were to become too wide, thus allowing lateral scattering and hence a possible channel for a reverse current, the effect of negative differential resistance will decrease.

In summary, we have presented initial evidence of a range of electronic instabilities associated with quantum reflections at a narrow channel when a sufficiently high bias is applied. Further aspects of the device potential, the theory and the effects of temperature and magnetic field will be published separately.

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